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EXAMINER	
RILEY, MARCUS T	

ART UNIT	PAPER NUMBER
2625	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,886	TAYLOR ET AL.	
	Examiner	Art Unit	
	MARCUS T. RILEY	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *2 and 4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, and 5-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/15/2006; 06/02/2009; 08/04/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application.
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 29, 2010 has been entered.

Response to Amendment

2. This office action is responsive to applicant's remarks received on July 29, 2010. **Claims 1, 3 & 5-7** and newly added **claims 8-12** are pending. **Claims 2 & 4** have been cancelled.

Response to Arguments

3. Applicant's arguments with respect to **claims 1, 3 & 5-7** and newly added **claims 8-12** have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claim 1** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the

invention. Claim 1 states in part *"each register having a type"*. It is not understood what the Applicant means by *"type"*. For continued examination purposes, Examiner has interpreted *"type"* to mean any type of register.

Even though the claimed subject matter did not appear to have adequate support in the Applicant's specification, the Examiner has tried to interpret the claims, as best the Examiner can ascertain, to develop an appropriate prior art rejection in the interests of compact prosecution. If any interpretation of the Examiner's is considered incorrect or off-base, the Examiner invites the Applicant to show the portions of the Applicant's specification which give a more proper interpretation of the claimed subject matter.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claim 1, 3 & 5-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Amini '538 et al. (US 5,381,538 hereinafter, Amini '538) in combination with Mills et al. (US 5,696,917 hereinafter, Mills '917) and Brown (US 6,029,239 hereinafter, Brown'239) as applied to claim 1, and further in view of Curry et al. (US 6,112,275 hereinafter, Curry '275).

Regarding claim 1; Amini '538 discloses a programmable interface comprising (Fig. 2, Planar I/O interface circuit 112, i.e. Planar I/O interface circuit provides PIO programming information to and receives PIO programming information from PIO registers 114. Column 7, lines 29-33):

a register file (Fig. 2, Register 104) having a plurality of registers (Fig. 2, 20 bytes of Register104), each register having a type (i.e. FIFO of register 104, Column 6, lines 40-58);

a run control register (Fig. 2, PIO Registers #114, i.e. PIO registers 114 store program information which is used during the operation of DMA controller 52. PIO registers include eight channels, corresponding to the eight channels of DMA controller 52. Each channel stores control information for a corresponding channel of DMA controller 52. Column 7, lines 35-40);

a Code Store SRAM (Fig. 1, SRAM 34) bidirectionally communicating with the microcontroller (Fig. 1, Microprocessor 30 i.e. SRAM 34 communicates with Microprocessor 30 as in Column 2, line 56 – thru column 3, line 3. The communication is bidirectionally per Column 3, lines 19-25);

a microcontroller configured to bidirectionally communicate with the register file and the run control register (i.e. Microprocessor #30 bidirectionally communicates DMA Controller 52 via bidirectional buffers 36 and 38. Because DMA Controller 52 includes register 104 & 114 as stated in Column 5, lines 35-45, the microcontroller configured to bidirectionally communicate with the register file and the run control register. See also Column 3, lines 19-25 and Column 2, line 56 thru column 3, line 3).

wherein the Code Store SRAM and the run control register bidirectionally communicates with a system processor (Fig. 1, Processor #20 i.e. Column 3, lines 19-25) that is external to the programmable interface (Fig. 2, Planar I/O interface circuit 112, i.e. Planar I/O interface circuit provides PIO programming information to and receives PIO programming information from PIO registers 114. Column 7, lines 29-33).

an external input/output (I/0) interface register, (Fig. 2, PIO Registers #114)

an internal I/0 register (i.e. FIFO of register 104, Column 6, lines 40-58)

a first-in, first-out (FIF0) register configured to communicate with a direct memory access (DMA) controller (i.e. FIFO of register 104, Column 6, lines 40-58);

Amini '538 does not expressly disclose an executable code, including one or more instructions; wherein the system processor is configured to load the executable code onto the

Code Store SRAM; and further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code; a general-purpose microcontroller register.

Mills '917 discloses and executable code, including one or more instructions (i.e. The program associated with the selected game will be loaded into SRAM 240. It is well know in the art that computer programs are made up of a large number of code instructions when executing the programs. Most of the memory address space will be read from to provide code instructions and data that infrequently changes. Column 9, lines 53-60 and Column 10, lines 33-53);

wherein the system processor (Fig. 2, Static Microprocessor 210) is configured to load the executable code onto the Code Store SRAM and further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code (Fig. 4. i.e. The program associated with the selected game will be loaded into SRAM 240 and programs executing from SRAM 240 can be accessed, and hence executed. The read cycle of Fig. 4 begins with the transition of output enable and chip enable signals from low voltage to high that enables the loading process. Column 10, lines 33-53, Column 12, lines 11-16 and Column 13, lines 42-67);

a general-purpose microcontroller register (Fig. 2, Static Microprocessor 210).

Amini '538 and Mills '917 are combinable because they are from same field of endeavor of communication systems (Mills '917 at *"Field of Invention"*).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Amini '538 by adding an executable code, loaded onto the Code Store RAM as taught by Mills '917. The motivation for doing so would have been because it advantageous to load the executable code in the SRAM to store the data so the data it will not be lost. Therefore, it would have been obvious to combine Amini '538 with Mills '917 to obtain the invention as specified in claim 1.

Amini '538 as modified does not expressly disclose shared registers or an interrupt register.

Brown '239 discloses a shared register (Fig. 3, DFP 320 and DSP i.e. DFP 320 and DSP share registers in data memory for control and status functions. Column 12, lines 34-44);

an interrupt register (Fig. 3, DFP 320 i.e. the DFP 320 incorporates the interrupt register - not shown. Column 19, lines 49-52)

Amini '538 and Brown '239 are combinable because they are from same field of endeavor of communication systems (Brown '239 at *"Field of Invention"*).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Amini '538 by adding registers as taught by Brown '239. The motivation for doing so would have been because it advantageous to have various registers to improve system architecture and enhance system performance. Therefore, it would have been obvious to combine Amini '538 with Brown '239 to obtain the invention as specified in claim 1.

Amini '538 as modified does not expressly disclose a timer register.

Curry '275 discloses a timer register (Fig. 21, Register 2104 i.e. Figures 22A-N are schematic circuit, timing, and state diagrams of the embodiment of Fig. 21. Column 36, lines 52-56).

Amini '538 and Curry '275 are combinable because they are from same field of endeavor of communication systems (Curry '275, See Title).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Amini '538 by adding the types of the registers as taught by Curry '275. The motivation for doing so would have been because it advantageous to provide several registers with higher functionality at lower cost in a more

compact package. Therefore, it would have been obvious to combine Amini '538 with Curry '275 to obtain the invention as specified in claim 1.

Regarding claim 3; Amini '538 as modified does not expressly disclose a programmable interface wherein the external I/O interface register includes an edge detect logic.

Curry '275 discloses a timer register a programmable interface wherein the external I/O interface register includes an edge detect logic (i.e. Fig. 9A-9B shows the control logic used in the registers. Column 15, lines 64-67 thru column 16, lines 1-13).

Amini '538 and Curry '275 are combinable because they are from same field of endeavor of communication systems (Curry '275, See Title).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Amini '538 by adding a register as taught by Curry '275. The motivation for doing so would have been because it advantageous to provide several registers with higher functionality at lower cost in a more compact package. Therefore, it would have been obvious to combine Amini '538 with Curry '275 to obtain the invention as specified in claim 1.

Regarding claim 6; Curry '275 discloses a programmable interface wherein the executable code is selected from a group that includes serial interfaces, parallel interfaces, serial peripheral interface (SPI), Synchronous Serial Interface (SSI), MicroWire, Inter Integrated Circuit (I2C), control area network (CAN), UART, IEEE1284, LCD interface, front panel interface, and MODEM (i.e. The programmable capabilities of the standard UART chip in the computer's RS232 interface are exploited to provide adaptation to the time base requirements of the module. Column 10, lines 18-28).

Regarding claim 7; Amini '538 discloses a programmable interface (Fig. 1, Bidirectional Buffers 36 & 38) wherein the system processor is configured to bidirectionally communicate with the

register file (i.e. Buffers 36, 38 are bidirectional and communicate with FIFO registers 104 in DMA. Column 3, lines 19-25 and Column 5, lines 35-45);

Regarding claim 8; Curry '275 discloses wherein the timer register is configured to (i) increment independently based on a selected system timebase, (ii) generate timing for protocols to be implemented, and (iii) detect protocol timeout errors (Fig. 21, Register 2104 i.e. Figures 22A-N are schematic circuit, timing, and state diagrams of the embodiment of Fig. 21. Column 36, lines 52-56).

Regarding claim 9; Amini '538 as modified does not expressly disclose wherein the shared register is accessed by both the system processor and the microcontroller, and wherein the shared register is configured to emulate a peripheral status, wherein an access priority grants write access to either the system processor or the microcontroller for accessing the to the shared register.

Brown '239 discloses wherein the shared register is accessed by both the system processor (Fig. 3, Digital Signal Processor, DSP 300) and the microcontroller (Fig. 3, Microcontroller Unit, MCU I/O 310), and wherein the shared register (Fig. 3, DFP 320 and DSP) is configured to emulate a peripheral status, wherein an access priority grants write access to either the system processor or the microcontroller for accessing the to the shared register (Fig. 3, DFP 320 and DSP i.e. DFP 320 and DSP share registers in data memory for control and status functions. Column 12, lines 34-44)

Amini '538 and Brown '239 are combinable because they are from same field of endeavor of communication systems (Brown '239 at *"Field of Invention"*).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Amini '538 by adding registers as taught by Brown '239. The motivation for doing so would have been because it advantageous to have various registers to improve system architecture and enhance system performance.

Therefore, it would have been obvious to combine Amini '538 with Brown '239 to obtain the invention as specified in claim 1.

Regarding claim 10; Amini '538 discloses wherein the external I/O interface register is configured to (i) facilitate the microcontroller to observe and control actual external electrical signals associated with a protocol of communications of the programmable interface, and (ii) facilitate implementation of a control state machine in the microcontroller (Fig. 2, PIO Registers #114 i.e. Planar I/O interface circuit 112 controls the transferring and storing of information in PIO registers 114 as well as DMA control backup circuit 110. Planar I/O interface circuit provides PIO programming information to and receives PIO programming information from PIO registers 114. Column 7, lines 29-40)

Regarding claim 11; Amini '538 discloses wherein the internal I/O register is configured to (i) facilitate an I/O subsystem to communicate with internal dedicated function blocks of the programmable interface (Fig. 3, DFP 320 i.e. FIFO register circuit 104, which is a 20-byte FIFO, performs a holding function for DMA controller 52. FIFO register circuit 104 allows for accumulating data so that the memory portion of a transfer can be aligned on a 16-byte packet boundary, thus allowing memory transfers to occur in 16-byte packet transfers. Column 6, line 59 thru Column 7, line 17).

Regarding claim 12; Brown '239 discloses wherein the interrupt register is configured to (i) facilitate an I/O subsystem to provide interrupt-driven status to the system processor (Fig. 3, DFP 320 i.e. DFP 320 contains hardware dedicated to interfacing with DSP's 300 interrupt routine and for memory access. Column 7, lines 16-31).

8. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Amini '538, Mills '917, Brown'239 and Curry '275 as applied to claim 1 above, and further in view of Ueda (US 5,631,637 hereinafter, Ueda '637).

Regarding claim 5; Amini '538 as modified does not expressly disclose a programmable interface wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page synchronization interface.

Ueda '637 discloses a programmable interface (Fig. 1, Main Control Unit 18) wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page synchronization interface (i.e. When the printing data of a page are developed in the bit map memory 17, the main control unit 18 sends a printing start signal 121 to a printing mechanism shown in Fig. 2. The printing mechanism is of so-called raster scanning type, such as a laser beam printer, and releases a horizontal synchronization (BD) signal 122 and a vertical synchronization signal 123 when the printing operation is enabled. Column 4, lines 7-14).

Amini '538 and Ueda '637 are combinable with because they are from same field of endeavor of communication systems (Ueda '637 at *"Field of Invention"*).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Amini '538 and Ueda '637 by adding a device wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page synchronization interface as taught by Ueda '637. The motivation for doing so would have been because it advantageous data to be processed faster and more efficiently. Therefore, it would have been obvious to combine Amini '538 with Ueda '637 to obtain the invention as specified in claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARCUS T. RILEY whose telephone number is (571)270-1581. The examiner can normally be reached on Monday - Friday, 7:30-5:00, est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David K. Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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